Curriculum Vitae

Patricio Carr

Bio Data

Name: Patricio Carr

Birth date: July 16th 1969

Residence: Simi Valley, CA, US

Contact Information:

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Technical Skills

- ASIC & FPGA digital design and verification. Verilog HDL, VHDL, Vera. Xilinx Foundation. Actel Libero. Synplicity. ModelSim. Chipscope.
- Embedded firmware development and verification. Micro assembly languages Motorola 68xx, Intel x86, Microchip PIC.
- High density PCB design.
- C, C++ programming. Scripting languages (Ruby, Perl, Python, bash/csh).
- Unix tools. GNU utilities (make, sed, awk, etc). Remote access (vnc, ssh, rsync, etc).
- Source code Revision Control Systems (CVS, SVN, SourceSafe).
- Linux systems installation & administration. Migration, interoperability, kernel compilation, emulation and virtualization.
- Web design & development. HTML, XHTML, CSS. Scripting PHP, Perl, SSI.

Education

College

Universidad Nacional de Rosario 03/1991 - 12/1992

Rosario, Argentina

Associates Degree in Computer Science. (Técnico Superior en Computación)

High School:

Instituto Politécnico Superior "General San Martín" 03/1983 - 12/1987

Rosario, Argentina

Work Experience

Contractor, FPGA design & verification 05/2005 to date

Innovative Integration Inc., Simi Valley, CA

- Worked on new and existing products adding features, debugging and customizing logic.
- Implemented interfaces with various IP cores.
  - 8-lane 250MHz PCI Express core based DMA engine on Xilinx Virtex5, sustained rate over 1GB/s.
  - PCI core interface for packet-based DMA engine streaming over 400MB/s sustained.
  - Virtual FIFO with 200 MHz DDR2 1Gbit backend memory.
  - Virtual FIFO with 100 MHz DDR 256Mbit backend memory.
  - 2 GHz dual lane RocketIO core.
- Written interfaces to several ADC & DAC chips up to 14-bit 400MS/s.
- Brought to spec-compliance FPDP interface.
- Interfaced with Texas Instruments DSPs TMS320C6713 & 6416 through EMIF, HPI.
- Designed 4-DSP high speed interconnecting mesh through 2 Virtex II-Pro FPGAs using RocketIO links.
- Interfaced with Texas Instruments DSPs TMS320C6713 & C6416 through EMIF & HPI. Written interfaces to SRAM, EEPROM & DRAM memories.
- Written module & top-level self-checking testbenches in VHDL & Verilog.

- Tools used: Xilinx ISE. PlanAhead. Modelsim MXE/SE/PE. Timing analysis. Xilinx Chipscope.
- Xilinx FPGAs: Spartan3E, Spartan2E, Virtex-II Pro and Virtex-5 parts. Coolrunner CPLD.
- Ported and automated implementation flow to run under Linux.
- Set up two new Linux servers to run source control, file & print server services.
- Implemented a wiki-style internal documentation system.
- Implemented an internal project management system.
- Set up a Subversion source control system with automated backup.

Consultant, VHDL debugging 01/2006

FO Engineering, Santa Clarita, CA

- Helped bring-up SPI design of a control/adquisition daughter board for water desalination system. Xilinx 9500XL CPLD. ISE7.1.

Contractor, VHDL design & verification 03/2005 - 05/2005

Inertial Airline Services Inc., Highland Heights, OH.

- Custom Ring-Laser-Gyro Test sets. Gyro Control Board. VHDL design.
- Debugged and fixed I2C interface implementation. Actel FPGA. Synplicity. Modelsim.

Contractor, VHDL design & verification 01/2005

Southwest Sciences Inc., Santa Fe, NM

- VHDL Design of additional features for a laser controller board.
- Added new features to existing product: A/D interfaces, Master & Slave SPI, PreAmps,
- Watchdog and Programmable Phase Clock. Actel FPGA. Synplicity. Modelsim.

Contractor, VHDL design & verification 11/2004 - 12/2004

Innovative Integration Inc., Simi Valley, CA

- Customized VHDL design of existing real time DSP-based capture board. Xilinx Spartan3 FPGA.
- Functional & Hardware verification of FPDP interface.

Contractor, VHDL verification 08/2004 - 09/2004

APK Engineering Inc., Westlake Village, CA

- Verification of real time A/D capture board. Xilinx Virtex II-Pro FPGA.
- Schematic implementation of VHDL top level.
- Web site redesign.

Employee, Sr. Digital Design Engineer 10/2001 - 07/2004

National Semiconductor Corp., Calabasas, CA

- Verilog & Vera verification of Ultra Low Power Gigabit Ethernet ASICs.
- Firmware design, verification and testing on software testbench and on actual silicon, for embedded 68HC11 processor. Implementation of new firmware features like programmable speed fallback under high error conditions.
- Vera environment. Main maintainer of testbench environment for several projects. Designed additions to testbench environment to ease verification approach. Ported simulation environment to several new related projects minimizing impact on simulation code. Testing and verification of testbench environment.
- Management of Perl, Ruby, shell scripts to run nightly regressions. In-house tools development.

Contractor, Digital Design Engineer 08/2000 - 10/2001

National Semiconductor Corp., Calabasas, CA

- Verilog verification of Ultra Low Power Gigabit Ethernet ASIC.
- Block and module level testing for datapath sub-system and DSP.
- Firmware design, testing and verification on software testbench. Traffic BIST firmware module implementation.
- RTL block module design and verification: variable depth multi-port datapath asynchronous FIFO.
- Vera environment. Enhanced simulation environment for easier porting to multi port design.
- Management of Perl/csh scripts to run sim regressions.

Contractor, PCB design 05/2000 - 10/2000

APK Engineering Inc., Agoura Hills, CA

- Designed 8 layer PCB for PCI-based board in OrCAD.
- FPGA, DSP and PCI bridge chips.

Employee, Firmware programming 07/1997 - 04/2000

Scanner Protection System SRL., Puerto Madryn, Argentina

- Design, testing, real-time emulation and verification of firmware code for Microchip's MCUs, using C and assembly for PICs.
- PCB design of most company's products, including alarm panels, remote controls, keyboards, etc.
- Design, development and deployment of company's home page.
- Graphic design of user's manuals and informative booklets.

Contractor, ASIC Verification 10/1996 - 04/1997

APK Engineering Inc., Agoura Hills, CA

- Central Processor Unit Redesign and Conversion into a FPGA.
- Schematic capture. Testbench design & development to verify state-of-the-art floating point microprocessor.
- Design of RAM behavioral models in HDL Verilog.
- Test and verification of microprocessor instructions, operating modes and peripherals.
- Pattern generation for arena screen project in C.
- Web site design & development.

Consultant, Software development 03/1988 - 07/1996

Several clients. Rosario, Argentina

- Design, development and testing of relational database systems for management. FoxPro, SQL.
- Design and development of minilab management system.
- HTML design and development. Graphic design and photo retouching.
- Device driver programming in C/C++. Assembly programming for low-level access to hard drives.

Part-time Computer Instructor 03/1995 - 6/1996

Colegio Normal Nro 1 (High school level). Entry level computing courses to students and adults. Offimatics.

Special Skills

Spoken languages:

- Spanish,
- English,
- Intermediate French, Alliance Francaise 04/2005-06/2006, Los Angeles,

Open Source Projects. `http://patocarr.com/linux/projects.shtml`

- Picasa-gen, xml parser with template-based html generator written in ruby, based on the output of Google Picasa.
- Pwiki, a collaborative tool for interactive document editing.
- Picblog, a ruby script used to download emails sent from a cell phone, directly onto a web page.
- Ipsaver, a perl script used to store/retrieve a client's dynamic IP from a static webpage.
- Free Software CD-ROM. Redesign of web interface of this argentinian free software project.

Attended seminars:

- Java Premier. LAX, CA. 12/1996
- Microchip Workshop '98. Buenos Aires, Argentina. 10/1998
- Microchip Workshop '99. Buenos Aires, Argentina. 10/1999
- Synopsys 2003 Synthesis and Timing workshop. Thousand Oaks, CA. 03/2003
- Novas Software. Debussy. Calabasas, CA. 08/2003.
- Wind River. Real-Time Linux solutions for embedded systems. Woodland Hills, CA. 07/2005